What is claimed is:

1. An I/O circuit placement method for placing I/O circuits included in a semiconductor device, comprising a step of:

placing at least two rows of I/O circuits on a first side of a chip, wherein each I/O circuit has a head section and a tail section, the placement direction of the head section and the tail section is perpendicular to that of the I/O circuits in the rows.

2. The placement method as claimed in claim 1 further comprises a step of placing another row of I/O circuits on a second side of the chip.

3. The placement method as claimed in claim 1, wherein the head sections are oriented to the tail sections in the adjacent rows.

4. The placement method as claimed in claim 1, wherein the head sections are oriented to the head sections in the adjacent rows.

5. The placement method as claimed in claim 1, wherein a different number of I/O circuits are placed in different rows.

6. A semiconductor device, comprising:

a chip; and

at least two rows of I/O circuits placed on a first side of the chip, wherein each I/O circuit has a head

section and a tail section, the placement direction of the head section and the tail section is perpendicular to that of the I/O circuits in the rows.

7. The semiconductor device as claimed in claim 6, further comprising another row of I/O circuits placed on a second side of the chip.

8. The semiconductor device as claimed in claim 6, wherein the head sections are oriented to the tail sections in the adjacent rows.

9. The semiconductor device as claimed in claim 6, wherein the head sections are oriented to the head sections in the adjacent rows.

10. The semiconductor device as claimed in claim 6, wherein the tail sections are oriented to the tail sections in the adjacent rows.

11. The semiconductor device as claimed in claim 6, further comprising a core circuit region disposed on the chip, wherein the rows of I/O circuits are disposed outside the core circuit region and are at the periphery of the chip.

12. The semiconductor device as claimed in claim 6, wherein the number of the I/O circuits placed in the different rows is different.

13. A semiconductor device, comprising:

a chip;

a core circuit region disposed on the chip;

a loop of I/O circuits disposed at the periphery of the chip and around the core circuit region; and

at least one row of I/O circuits disposed between the loop of I/O circuits, wherein each I/O circuit has a head section and a tail section, the placement direction of the head section and the tail section is perpendicular to that of the I/O circuits in the loop or the row.

14. The semiconductor device as claimed in claim 13, wherein the head sections are oriented to the tail sections in the adjacent rows.

15. The semiconductor device as claimed in claim 13, wherein the head sections are oriented to the head sections in the adjacent rows.

16. The semiconductor device as claimed in claim 13, wherein the tail sections are oriented to the tail sections in the adjacent rows.